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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/681,125	10/09/2003	Shih-Fang Chen	0941-0849P	8072

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EXAMINER	
SARKAR, ASOK K	

ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 06/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/681,125	CHEN, SHIH-FANG	
	Examiner	Art Unit	
	Asok K. Sarkar	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 May 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) *22-24* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election with traverse of Group I claims 1 - 21 in the reply filed on May 17, 2004 is acknowledged.

2. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

3. Claims 22 – 24 were withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected group II claims, there being no allowable generic or linking claim. Election was treated as made **without** traverse in the reply filed on May 17, 2004.

Claim Objections

4. Claim 1 is objected to because of the following informalities: In line 10, the word "exposed" should be replaced by "above". In line 11, the word "reveal" should be replaced by "cover". In line 17, the word "forming" should be replaced by "form". In line 19, the word "resulted" should be replaced by "resulting". Appropriate correction is required.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 15, 18, 20 and 21 are rejected under 35 U.S.C. 102(b) as being anticipated by Radens, US 6,265,279.

Regarding claim 15, Radens teaches a trench capacitor process for preventing parasitic leakage, capable of blocking leakage current resulting from a parasitic transistor adjacent to the trench, comprising the steps of:

- forming a doping layer 220 and a cap layer 222 covering part of the sidewall of the trench 206 (see Fig. 8) in between column 5, line 25 and column 6, line 44; and
- performing an annealing process (column 6, line 12) on the doping layer and forming a dopant region in the substrate adjacent to the sidewall of the trench to block leakage current resulting from a parasitic transistor adjacent to the trench in column 6, lines 61 - 67.

Regarding claim 18, Radens teaches a trench capacitor wherein the charging conductivity of the dopants (positive dopants in column 5, line 37) in the doping region is the same as that in the p-substrate (column 4, line 66).

Regarding claim 20, Radens teaches a trench capacitor wherein the dopant region does not contact the surface of the substrate and has a first distance therebetween with reference to Fig. 8.

Regarding claim 21, Radens teaches a trench capacitor wherein the first distance is about 500 – 2500 Å in column 5, line 23.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

9. Claims 1 – 6, 10 – 12 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Radens, US 6,265,279.

Regarding claim 1, Radens teaches A trench capacitor- process for preventing parasitic leakage, comprising the steps of:

- providing a substrate 202 with a trench 206 formed therein, wherein the trench has a buried plate 209 formed adjacent to the lower portion thereof (see Fig. 2);
- forming a dielectric layer 208 and a first conductive layer 210 in the lower portion of the trench, wherein the buried plate 209 and the first conductive layer 210 are separated by the dielectric layer 208 (see Fig. 2);
- forming a doping layer 220 on portions of each sidewall of the trench exposed by the dielectric layer 208 and the first conductive layer 210 to cover portions of sidewalls 214 of the trench in the upper portion (see Fig. 3);
- forming a cap layer 222 on each exposed sidewall and each doping layer 220 (see Fig. 7);

- performing an annealing process on each doping layer to forming a dopant region in the adjacent substrate in column6, lines 12 - 13, wherein each dopant region blocks leakage current resulted from a parasitic transistor adjacent to the trench and has a first distance from the surface of the substrate with reference to Fig. 7 in his general descriptions provided in columns 4 – 6;

Radens teaches filling up the rest of the trench with conductive layers that has substantially the same height with respect to the dopant regions; removing portions of the cap layers exposed by the conductive layer to reveal portions of the sidewalls in the upper portion of the trench; and continuing with the same third conductive layer on the second conductive layer to fill the trench, wherein the third conductive layer directly contacts the exposed sidewalls in the upper portions of the trench with respect to Fig. 8, but fails to expressly teach the steps of forming a second conductive layer in the trench to expose portions of the cap layers, wherein the second conductive layer contacts the first conductive layer and has substantially the same height with respect to the dopant regions; removing portions of the cap layers exposed by the second conductive layer to reveal portions of the sidewalls in the upper portion of the trench; and forming a third conductive layer on the second conductive layer to fill the trench, wherein the third conductive layer directly contacts the exposed sidewalls in the upper portions of the trench.

However, it would have been obvious to one with ordinary skill in the art at the time of the invention to modify radens and follow the above-mentioned steps of forming a second conductive layer in the trench to expose portions of the cap layers, wherein

the second conductive layer contacts the first conductive layer and has substantially the same height with respect to the dopant regions; removing portions of the cap layers exposed by the second conductive layer to reveal portions of the sidewalls in the upper portion of the trench; and forming a third conductive layer on the second conductive layer to fill the trench, wherein the third conductive layer directly contacts the exposed sidewalls in the upper portions of the trench since these steps will be necessary in order to complete the device fabrication by Radens as shown in Fig. 8 especially if the second and third conductive layers are filled with the same n-doped polysilicon material as the bottom material for the capacitor.

Regarding claim 2, Radens teaches p-substrate in column 4, line 66.

Regarding claims 3 and 4, Radens teaches a dielectric material of silicon nitride in column 5, lines 12 – 14.

Regarding claim 5, Radens teaches buried plate of n-doped region in column 2, lines 14 – 15.

Regarding claim 6, Radens teaches the conductive material inside the trench 210 as n-type polysilicon in column 5., line 15.

Regarding claim 10, Radens teaches the trench capacitor wherein the doping region is vertically distributed in the substrate adjacent to the trench and approximately equidistant from the trench with reference to Fig. 8.

Regarding claim 11, Radens teaches the annealing process is furnace annealing in column 6, line 12.

Regarding claims 12 and 14, Radens teaches the limitations as explained earlier in rejecting claims 18 and 21.

10. Claims 7, 9, 13, 17 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Radens, US 6,265,279 as applied to claims 1 and 15 above, and further in view of Mandelman, US 6,163,045.

Regarding claims7, 9 and 17, Radens fails to teach n-doped polysilicon as As-doped and the cap layer a s silicon oxide.

Mandelman teaches a trench capacitor in which they teach n-doped polysilicon as As-doped and the cap layer a s silicon oxide as conventional and well known art in column 3, lines 25 – 54.

Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention to modify Radens and use n-doped polysilicon as As-doped and the cap layer a s silicon oxide as they are conventional and well known art taught by Mandelman in column 3, lines 25 – 54.

Regarding claims 13 and 19, Radens fails to teach the doping level of the substrate and the doping region.

Mandelman teaches doping range for the doping region (column 3, line 64) to be about double of that of the substrate (column 3, line 46) for the benefit of reduced leakage current and thinner collar in column 3, lines 61 – 67.

Therefore, it would have been obvious to one with ordinary skill in the art at the

time of the invention to modify Radens and use a doping range for the doping region to be about double of that of the substrate for the benefit of reduced leakage current and thinner collar as taught by Mandelman in column 3, lines 61 – 67.

11. Claims 8 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Radens, US 6,265,279 as applied to claims 1 and 15 above, and further in view of Becker, US 4,782,036.

Radens fails to teach doping layer as a borosilicate glass.

Becker teaches doping trenches with borosilicate glass for the benefit of doping by a process that is simple, rapid and self adjusting compared to that of ion implantation in between column 1, line 7 and column 2, line 20.

Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention to modify Radens and use borosilicate glass for doping for the benefit of doping by a process that is simple, rapid and self adjusting compared to that of ion implantation as taught by Becker in between column 1, line 7 and column 2, line 20.

Conclusion

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Asok K. Sarkar whose telephone number is 571 272 1970. The examiner can normally be reached on Monday - Friday (8 AM- 5 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kammie Cuneo can be reached on 571 272 1957. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

13. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Asok K. Sarkar
June 10, 2004

Patent Examiner